13. (Amended) A semiconductor integrated circuit as set forth in claim 12, which further comprises a third capacitor element provided between the drain terminal and the source terminal of said FET,

wherein a capacitance value of said third capacitor element is set so that a parasitic resistance component of said FET decreases when the drain voltage of said FET is lower than the source voltage thereof.

REMARKS

Favorable reconsideration of the application is respectfully requested in light of the foregoing amendments and following discussion.

Claims 1-20 are presently pending. Claims 2-6, 12 and 13 are amended herein.

The outstanding Official Action includes: (i) an objection to material incorporated by reference into the application; (ii) an objection to the drawings; (iii) a rejection of Claims 2-6 and 14-16 under 35 U.S. §112, second paragraph; (iv) a rejection of Claims 11, 13, 14, 16-18 and 20 under 35 U.S. §102(b) in view of U.S. Patent No. 4,696,639 ("Bohan"); (v) a rejection of Claims 1-10 under 35 U.S. §102(b) in view of U.S. Patent 4,454,485 ("Fisher"); and (vi) an indication of allowable subject matter in Claims 12, 15 and 19.

Applicants acknowledge with appreciation the indication of allowable subject matter in Claims 12, 15 and 19. It is respectfully submitted that all claims are allowable, for at least the reasons set forth herein.

Regarding the objection to material incorporated by reference, it is respectfully submitted that the essential matter of the present invention is properly disclosed in the present specification, and the present application does not rely on improper incorporation by reference of essential material from other references. Accordingly, withdrawal of the rejection is respectfully requested.

The Office Action includes objections to the drawings. A Letter Requesting Approval of Drawing Changes is being filed in conjunction with this Amendment attending to the objections to the drawings. Accordingly, withdrawal of the objections to the drawings is respectfully requested.

The Office Action includes a rejection of Claims 2-6 and 14-16 under 35 U.S. §112, second paragraph, for various informalities. The present Amendment includes amendments to each of Claims 2-6 and 14-16 to comply with the Office Action and address these informalities. Accordingly, withdrawal of the rejection is respectfully requested.

The rejection of Claims 11, 13, 14, 16-18 and 20 under 35 U.S. §102(b) in view of Bohan is respectfully traversed.

In the present claims 11-20, when the drain voltage of the FET is lower than the source voltage of the FET, the inductance element connected between the source of the FET and the ground terminal is subjected to series resonance for the reactance component of the impedance between the gate and source of the FET. Therefore, it is possible to sufficiently reduce the amount of current for transmitting the signal when the FET is OFF, thereby reducing power consumption of the semiconductor integrated circuit.

The oscillator 20 of the Bohan patent includes the FET 21 and the inductor 28. The capacitor 26 is connected in series between the source of the FET 21 and the ground terminal. The inductor of Bohan is a component constituting a portion of the oscillator, and is not subjected to series resonance for the reactance component of the impedance between the gate and the source of the FET.

Bohan does not disclose, or even suggest, how to set the inductance value of the inductor 28 and the above-mentioned series resonance. The Bohan patent does not realize advantageous effects of the present invention, such as reducing the amount of current for transmitting the signal in the case when the drain voltage of the FET is lower than the source

voltage of the FET. Accordingly, it is respectfully submitted that one of ordinary skill in the art would not have conceived the inductor element of the claimed invention based on the description of Bohan. Consequently, the Bohan patent does not disclose "wherein an inductance value of said inductor element is set so that said inductor element resonates in series for a reactance component of a gate-to-source impedance by said controlled signal when a drain voltage of said FET is lower than a source voltage thereof," as recited in Claim 11.

Accordingly, the Bohan patent does not disclose features of the claimed invention. Therefore, withdrawal of the rejection of Claims 11, 13, 14, 16-18 and 20 under 35 U.S. §102(b) is respectfully requested.

The rejection of Claims 1-10 under 35 U.S. §102(b) in view of Fisher is respectfully traversed.

In claims 1-10, when the drain voltage of the FET is lower than the source voltage, the inductor element connected between the source terminal of the FET and the ground terminal is subjected to series resonance for the reactance component of the impedance between the gate and the source of the FET.

An oscillation circuit having the inductor 17 connected between the source of the FET and the ground terminal is depicted in Figure 1 of the Fisher patent. However, Fisher does not disclose, or even suggest, the series resonance for the reactance component of the impedance between the gate and the source of the FET, nor how to decide the inductance value of the inductor 17. Accordingly, it is respectfully submitted that one of ordinary skill in the art would not have conceived the inductor element of the claimed invention based on the description of Fisher. Consequently, the Fisher patent does not disclose "wherein an inductance value of said inductor element is set so that said inductor element resonates in series for a reactance component of a gate-to-source impedance by said controlled signal

when a drain voltage of said FET is lower than a source voltage thereof," as recited in Claim 1.

Accordingly, the Fisher patent does not disclose features of the claimed invention. Therefore, withdrawal of the rejection of Claims 1-10 under 35 U.S. §102(b) is respectfully requested.

In light of the above, it is respectfully submitted that the claimed invention is patentably distinguishable from the applied patents. Since no further issues are outstanding and the application is believed to be in condition for allowance, an early and favorable action is respectfully requested. In the event that issues arise in the application which could readily be resolved by telephone, the Examiner is kindly invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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IN THE CLAIMS

Please amend claims 2-6, 12 and 13 as follows.

2. (Amended) A semiconductor integrated circuit as set forth in claim 1, which further comprises a [second] first capacitor element provided between the gate terminal and the source terminal of said FET,

wherein a capacitance value of said [second] first capacitor element is set so that a parasitic resistance component of said FET [apparently] decreases when the drain voltage of said FET is lower than the source voltage thereof.

3. (Amended) A semiconductor integrated circuit as set forth in claim 1, which further comprises a [third] second capacitor element provided between the drain terminal and the source terminal of said FET,

wherein a capacitance value of said [third] second capacitor element is set so that a parasitic resistance component of said FET [apparently] decreases when the drain voltage of said FET is lower than the source voltage thereof.

4. (Amended) A semiconductor integrated circuit as set forth in claim 1, which further comprises a control signal input circuit, connected to the drain terminal of said FET, configured to [switch and controlling the] control a magnitude relationship between the drain voltage and the source voltage of said FET.

5. (Amended) A semiconductor integrated circuit as set forth in claim 2, which further comprises a control signal input circuit, connected to the drain terminal of said FET, configured to [switch and controlling the] control a magnitude relationship between the drain voltage and the source voltage of said FET.

6. (Amended) A semiconductor integrated circuit as set forth in claim 3, which further comprises a control signal input circuit, connected to the drain terminal of said FET, configured to [switch and controlling the] control a magnitude relationship between the drain voltage and the source voltage of said FET.

12. (Amended) A semiconductor integrated circuit as set forth in claim 11, which further comprises a second capacitor element provided between the gate terminal and the source terminal of said FET,

wherein a capacitance value of said second capacitor element is set so that a parasitic resistance component of said FET [apparently] decreases when the drain voltage of said FET is lower than the source voltage thereof.

13. (Amended) A semiconductor integrated circuit as set forth in claim [11] 12, which further comprises a third capacitor element provided between the drain terminal and the source terminal of said FET,

wherein a capacitance value of said third capacitor element is set so that a parasitic resistance component of said FET [apparently] decreases when the drain voltage of said FET is lower than the source voltage thereof.